



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,837	10/30/2003	Li-Chyn Wang	MSCP0016USA	2836
27765	7590	06/16/2006	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION			TRAN, VINCENT HUY	
P.O. BOX 506			ART UNIT	
MERRIFIELD, VA 22116			PAPER NUMBER	

2115

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/605,837

Applicant(s)

WANG, LI-CHYN

Examiner

Vincent T. Tran

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 7-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 7-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Action is responsive to the communication filed on 3/30/06.
2. Claims 1-5, 7-9 are pending for examination.
3. Claims 6, 10-16 are cancelled.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki U.S. Patent 5,995,454 in view of Touchet US 20030221093.

8. As per claim 1, Yamaki discloses a method for enabling a computer to self-start comprising:

Art Unit: 2115

selecting a predetermined time for self-start when the computer is on [col. 4 lines 19-28];
adjusting an alarm setting stored in a memory of an RTC/NVRAM chip according to the predetermined time [col. 4 lines 36-47; col. 5 lines 35-37; col. 6 lines 51-59];
powering the computer off [col. 5 lines 33-34]; and
providing electrical power with a power supply if a clock value of the RTC/NVRAM chip matches the alarm setting [col. 4 lines 47-52];
sending a power on signal to the power supply via the power supply connector on the motherboard [col. 4 lines 48-52];
and starting the computer [col. 7 lines 14-21].

However, Yamaki does not explicitly teach the powering of the voltages of pins of the power supply connector to appropriate levels;

checking if the voltage in the pins of the power supply connector are stable;
sending a power good signal from the power supply to a processor of the computer.

Touchet teaches another method relates to the initialization of a computer system.

Specifically, Touchet teaches

powering of the voltages of pins of the power supply connector to appropriate levels;
checking if the voltage in the pins of the power supply connector are stable;
sending a power good signal from the power supply to a processor of the computer; and
stating the computer upon receiving the power good signal [paragraph 0026].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Yamaki with the detecting of the power good

signal from the power supply before power on the computer of Touchet in order to prevent possible damage to the system.

9. **Note:** The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Haider US 200400644747.

powering of the voltages of pins of the power supply connector to appropriate levels;
checking if the voltage in the pins of the power supply connector are stable;
sending a power good signal from the power supply to a processor of the computer; and
stating the computer upon receiving the power good signal [paragraph 0017, 0019].

10. Claims 2-3, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki as applied to claim 1 above, and further in view of Lin et al. US 20030095044.

11. As per claim 2, Yamaki teaches the enabling the power supply controller (PSC) wherein the PSC chipset is able to respond to a matching signal send from the RTC/NVRAM chip when the computer is off [col. 4 lines 47-52]. However, Yamaki does not teach enabling the system control interrupt bit in a Southbridge chip set of the computer.

Lin et al. teach another method that enabling the computer to turned on via a wireless remote controller. Specifically, Lin et al. teach enabling the System Control Interrupt (SCI) bit in a Southbridge chip set of the computer; wherein the Southbridge chipset is able to respond to a matching signal sent from a wireless remote controller when the computer is off [paragraph 0026 and 0027].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Yamaki with the Southbridge of Lin et al. since the Southbridge chipset is well know the art of computer architect.

12. Claims 1, 4, 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomiyasu U.S. Patent 6,134,187.

13. As per claim 1, Tomiyasu discloses a method for enabling a computer to self-start comprising:

- selecting a predetermined time for self-start when the computer is on [fig. 9; col. 6 lines 42-48];

- adjusting an alarm setting stored in a memory of an RTC/NVRAM chip according to the predetermined time [col. 6 lines 49-53];

- powering the computer off [inherent]; and

- providing electrical power with a power supply if a clock value of the RTC/NVRAM chip matches the alarm setting [col. 7 lines 3-20];

- sending a power on signal to the power supply via a power supply connector on a motherboard of the computer; and

- starting the computer.

However, Tomiyasu does not explicitly teach

- powering of the voltages of pins of the power supply connector to appropriate levels;

- checking if the voltage in the pins of the power supply connector are stable;

- sending a power good signal from the power supply to a processor of the computer; and

stating the computer upon receiving the power good signal.

Touchet teaches another method relates to the initialization of a computer system.

Specifically, Touchet teaches

powering of the voltages of pins of the power supply connector to appropriate levels;

checking if the voltage in the pins of the power supply connector are stable;

sending a power good signal from the power supply to a processor of the computer; and

stating the computer upon receiving the power good signal [paragraph 0026].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Tomiyasu with the detecting of the power good signal from the power supply before power on the computer of Touchet in order to prevent possible damage to the system.

14. As per claim 4, Tomiyasu discloses sending a matching signal from the RTC/NVRAM chip by changing the value of the 11th byte in the memory of the RTC/NVRAM chip [col. 5 lines 46-57 – see fig. 6 for byte position].

15. As per claim 7, Tomiyasu discloses using an application of an operating system in the computer to select the predetermined time [fig. 9].

16. As per claim 8, Tomiyasu discloses the operating system employs a driver to relay the selected predetermined time to the BIOS [inherent - col. 6 lines 49-53; col. 3 lines 47-49].

17. As per claim 9, Tomiyasu discloses the adjusting of the alarm setting further comprises:
employing the BIOS to adjust the alarm setting in the memory of the RTC/NVRAM chip
[col. 6 lines 49-53; col. 3 lines 47-49].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Tran


CHUN CAO
PRIMARY EXAMINER